METHOD OF MAKING A finFET HAVINGSUPPRESSED PARASITIC DEVICE CHARACTERISTICS

Abstract

A finFET (100) having sidwall spacers (136, 140) to suppress parasitic devices in the upper region of a channel and at the bases of source(s) and drain(s) that are artifacts of the fabrication techniques used to make the finFET. The FinFET is formed on an SOI wafer (104) by etching through a hardmask (148) so as to form a freestanding fin (120). Prior to doping the source(s) (124) and drain(s) (128), a layer (156) of thermal oxide is deposited over the entire finFET. This layer is etched away so as to form the sidewall spacers at each reentrant corner formed where a horizontal surface meets a vertical surface. Sidewall spacers (136) inhibit doping of the upper region of source(s) and drain(s) immediately adjacent the gate. Sidewall spacers (140) fill in any undercut regions (144) of BOX layer (116) that may have been formed during prior fabrication steps.